UM10064

ISP1181x Microcontroller Eval Kit

Rev. 01 — 15 February 2007 **User manual**

Document information

Info	Content
Keywords	isp1181a, isp1181b, usb, universal serial bus, peripheral
Abstract	This document explains the ISP1181x microcontroller eval kit. This kit enables you to evaluate the ISP1181x, and also perform firmware and product prototype development. **Remark**: The file name of the previous revision is 1181_MCU_EVAL_KIT_MANUAL-01.pdf. **Remark**: ISP1181x denotes the ISP1181A and the ISP1181B, and any future derivative.

Revision history

Rev	Date	Description
01	20070215	First release.

Contact information

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Remark: ISP1181x denotes the ISP1181A and the ISP1181B, and any future derivative.

1. Introduction

The ISP1181x is a full-speed cost-optimized and feature-optimized Universal Serial Bus (USB) Peripheral Controller with up to 14 configurable endpoints. It has a high-speed general-purpose parallel interface to communicate with many types of microcontrollers or microprocessors. It supports bus configurations and local Direct Memory Access (DMA) transfers of up to 16 bytes per cycle.

To a microcontroller, the ISP1181x appears as a memory device with an 8-bit or 16-bit data bus and a 1-bit address bus. The ISP1181x supports both multiplexed and nonmultiplexed address and data bus.

The ISP1181x can also be configured as a DMA slave device to allow more efficient data transfer. One of the 14 endpoint FIFOs may directly transfer data to or from the local shared memory.

Feature evaluation of the ISP1181x, firmware and product prototype development can easily be done with this set up. The ISP1181x microcontroller evaluation (eval) kit comes with the ISP1181x, microcontroller boards, test application program, USB driver, and sample firmware source codes. The firmware provided with the kit is written in the C language, allowing you to port it to other platforms for compilation. With this kit, you can develop your USB peripherals through firmware and hardware schematics.

2. System requirements

Running the kit only requires a new-generation PC, motherboard with the USB port, with Microsoft Windows 98 or Windows 2000 operating system.

3. Jumper settings on the ISP1181x board

Jumpers JP1 and JP2 set bus configuration mode of the ISP1181x. Table 1 shows Mode 2 of the bus configuration as the default setting.

Table 1. Default setting for the bus configuration – JP1 and JP2

Jumper number	Default setting
JP1	Short pins 1 and 2
JP2	Short pin 2 and 3

Jumpers JP3 and JP4 are for debugging. When used, all the signals from the ISP1181x can be propagated. For the JP3 and JP4 pin outs, see Section 7.

Table 2. Default setting for the bus configuration – JP4

Jumper number	Default setting
JP4	Short pin 19 and 20

The ISP1181x has four bus configuration modes, selected using pins BUS_CONF1 and BUS_CONF0:

Mode 0: 16-bit I/O port shared with the 16-bit DMA port

Mode 1: reserved

Mode 2: 8-bit I/O port shared with the 8-bit DMA port

Mode 3: reserved

Table 3 shows the bus configuration for each of these modes.

Table 3. Bus configuration modes

Mode	BUS_CONF[1:0]	PIO data width	DMA data width (DMAWD = 0)	DMA data width (DMAWD = 1)
0	00	DATA[15:0], 16-bit	-	16-bit on D[15:0] = DMA DATA[15:0]
1	01	reserved	reserved	reserved
2	10	DATA[7:0], 8-bit	8-bit on D[7:0] = DMA DATA [7:0]	-
3	11	reserved	reserved	reserved

4. Pin signal information of connectors

The connection between the ISP1181x microcontroller board and the ISP1181x board is through a 40-pin connector on the ISP1181x microcontroller board (JP3) and the ISP1181x board (JP8), respectively. Table 4 shows the pin description of JP3 and JP8.

Table 4. Pin description for JP3 and JP8

Pin	Type	Description
1	Power	V_{CC}
2	Power	V_{CC}
3	I/O	DATA0
4	I	ISP1181x EOT
5	I/O	DATA1
6	O	ISP1181x DREQ: This line is an asynchronous channel request used by the peripheral to gain DMA service. Bringing the DRQ line to active HIGH generates a DMA request.
7	I/O	DATA2
8	I	ISP1181x DACK: This line is used to acknowledge the DMA request and is active LOW.
9	I/O	DATA3
10	Power	ISA-5V
11	I/O	DATA4
12	Power	ISA-5V
13	I/O	DATA5
14	I	ISP1181x CS#
15	I/O	DATA6
16	I	ISP1181x WR#: This command line instructs an I/O device to read data on the data bus. The processor or the DMA controller may drive it. This signal is active LOW.

Pin	Type	Description
17	I/O	DATA7
18	I	ISP1181x RD#: This command line instructs an I/O device to drive its data on the data bus. The processor or the DMA controller may drive it. This signal is active LOW.
19	I/O	DATA8
20	I	ISP1181x WAKEUP
21	I/O	DATA9
22	O	ISP1181x READY
23	I/O	DATA10
24	O	ISP1181x SUSPEND
25	I/O	DATA11
26	O	ISP1181x INT: This line is rising edge-triggered. Raising this line HIGH and holding until the processor acknowledges it generates an interrupt request.
27	I/O	DATA12
28	Power	GND
29	I/O	DATA13
30	I	ALE
31	I/O	DATA14
32	Power	GND
33	I/O	DATA15
34	I	ISP1181x RESET#
35	Power	GND
36	Power	GND
37	I	ISP1181x A0
38	O	ISP1181x CLKOUT
39	Power	GND
40	Power	GND

5. Installation of hardware, firmware, INF and driver

1. Connect JP3 on the ISP1181x microcontroller board to JP8 on the ISP1181x board.
2. Connect the USB cable between J1 on the ISP1181x board and the host PC.
3. If it is the first time that the eval board is connected to the host PC, the host operating system Device Manager will prompt for the installation of INF and driver.

4. Select the location of D13TEST.INF and D13TEST.SYS from the ISP1181x evaluation CD, and complete the installation procedure. D13TEST.INF and D13TEST.SYS are located under “ISP1181 MCU Driver (Win98&2K) – Ver1.1.zip.” After unzipping files, run the “ISP1181 MCU Driver (Win98&2K) – Ver1.1.exe” and click through the install shield process to successfully install the driver on your PC. The default installation directory is “C:\Program Files\NXP\ISP1181 MCU Driver(Win98_2K) – Ver1.1.”

6. Using the host applet

Test applet D13TEST.EXE exercises all ISP1181x endpoints as shown in Fig 1.

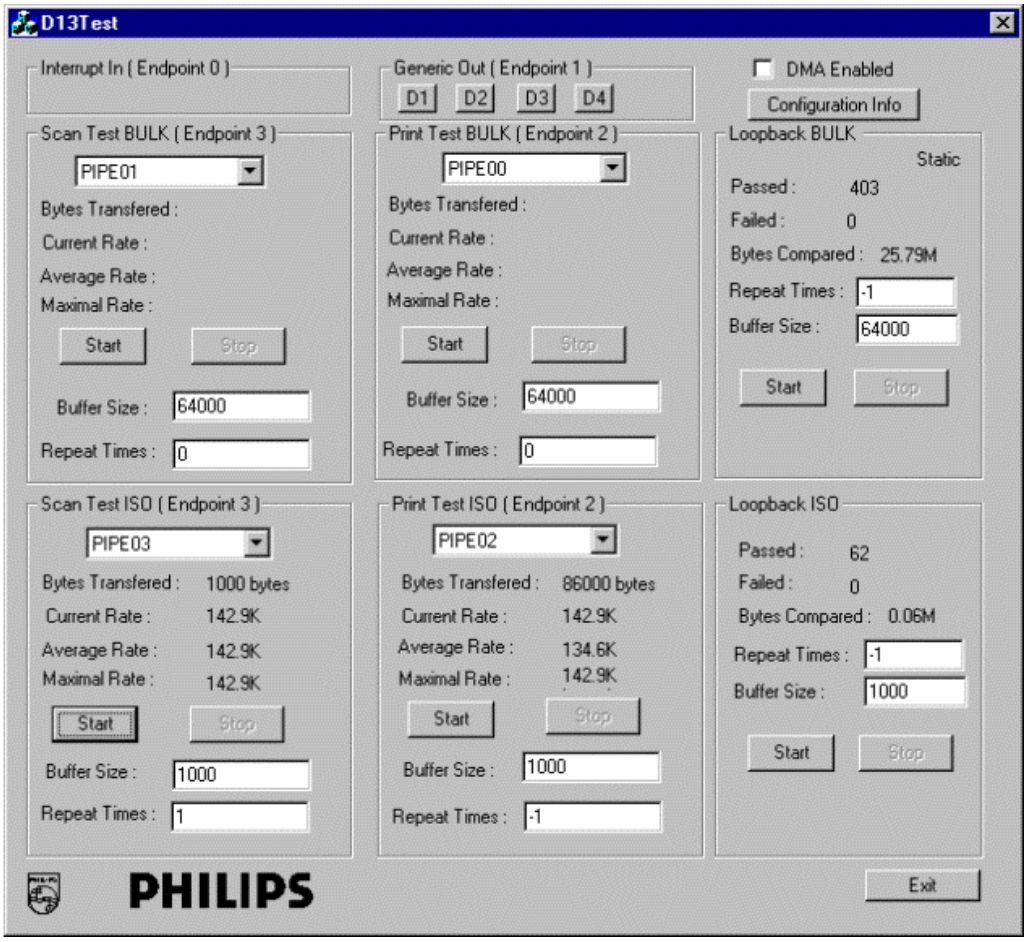

Fig 1. Applet D13TEST

Further testing of control endpoints can be done using standard USB Chapter 9 test programs. Table 5 describes the endpoint operations on the ISP1181x eval board.

Table 5. Description of endpoint operations

The test applet and the ISP1181x eval board support three test modes: loopback, print and scan. The firmware uses I/O accesses on this endpoint

Endpoint number	Endpoint type	Operations
1	ISO-OUT	This pipe is defined as an isochronous OUT pipe.
2	ISO-IN	This pipe is defined as an isochronous IN pipe.
3	Bulk-OUT	This pipe is defined as a bulk OUT pipe.
4	Bulk-IN	This pipe is defined as a bulk IN pipe.

Three test modes:

- **Scan mode**: In this mode, the ISP1181x eval board acts like a scanner. It sends data packets to the host PC as fast as possible. Use this mode to evaluate the isochronous IN and bulk IN transfer rates.
- **Print mode**: In this mode, the ISP1181x eval board acts like a printer. It receives data packets from the host PC as fast as possible. Use this mode to evaluate the isochronous OUT and bulk OUT transfer rates.
- **Loopback mode**: In this mode, the ISP1181x eval board receives data packets on the isochronous OUT or bulk OUT endpoint and sends them back to the host PC on the isochronous IN or bulk IN endpoint. Use this mode to test the data integrity of transfers.

The Buffer Size setting on the test applet is determined by firmware and hardware capability of the eval board. For the microcontroller eval kit, the maximum size is limited to 64000 for the bulk transfer.

Remark: The **DMA Enabled** checkbox in the upper-right corner of D13TEST must be enabled.

Repeat Times for the loopback test controls the numbers of iterations of loopback, which is useful for debugging. To run the test infinite times, set Repeat Times as –1.

7. Schematics

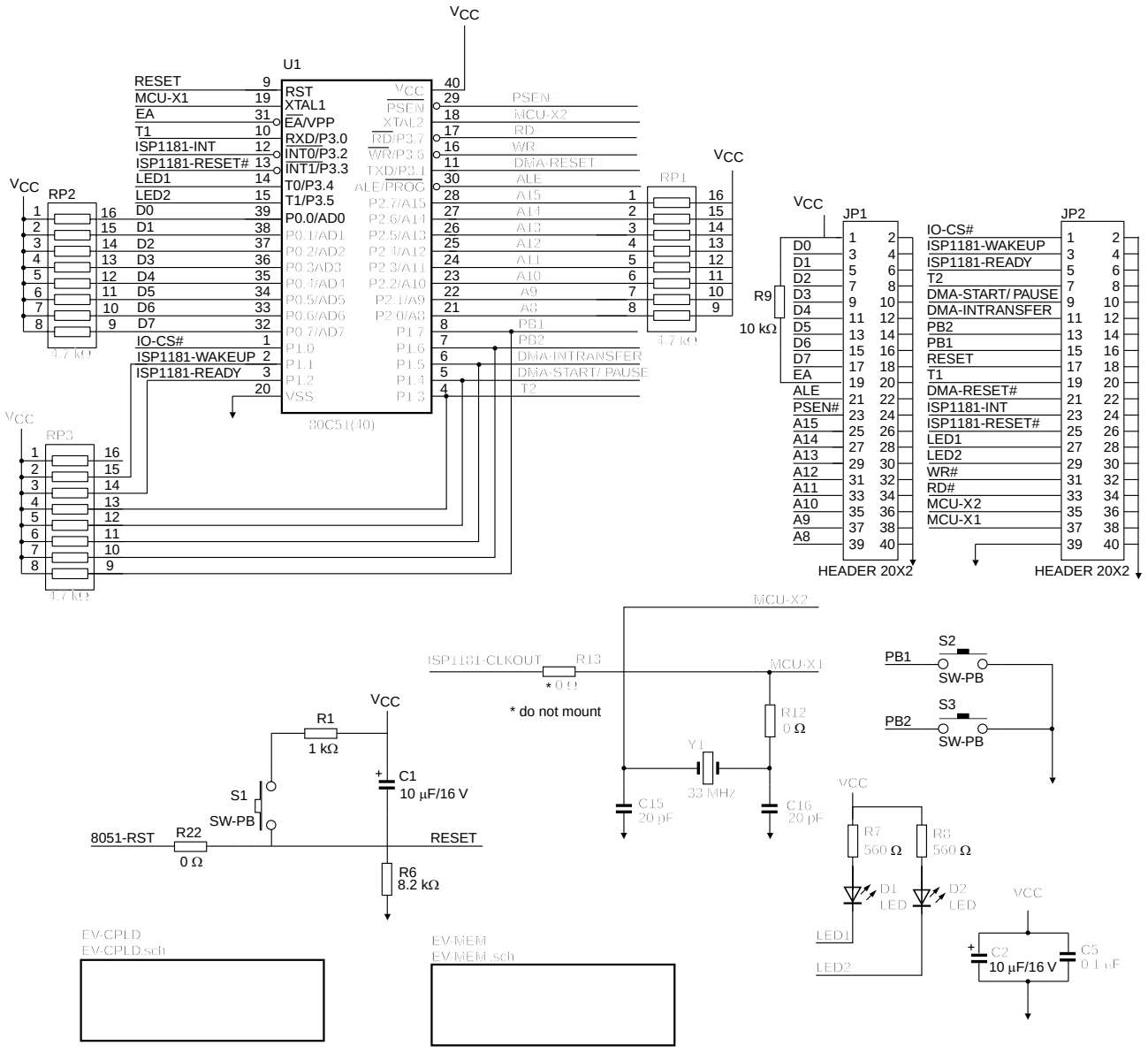

Fig 2. Schematics 1

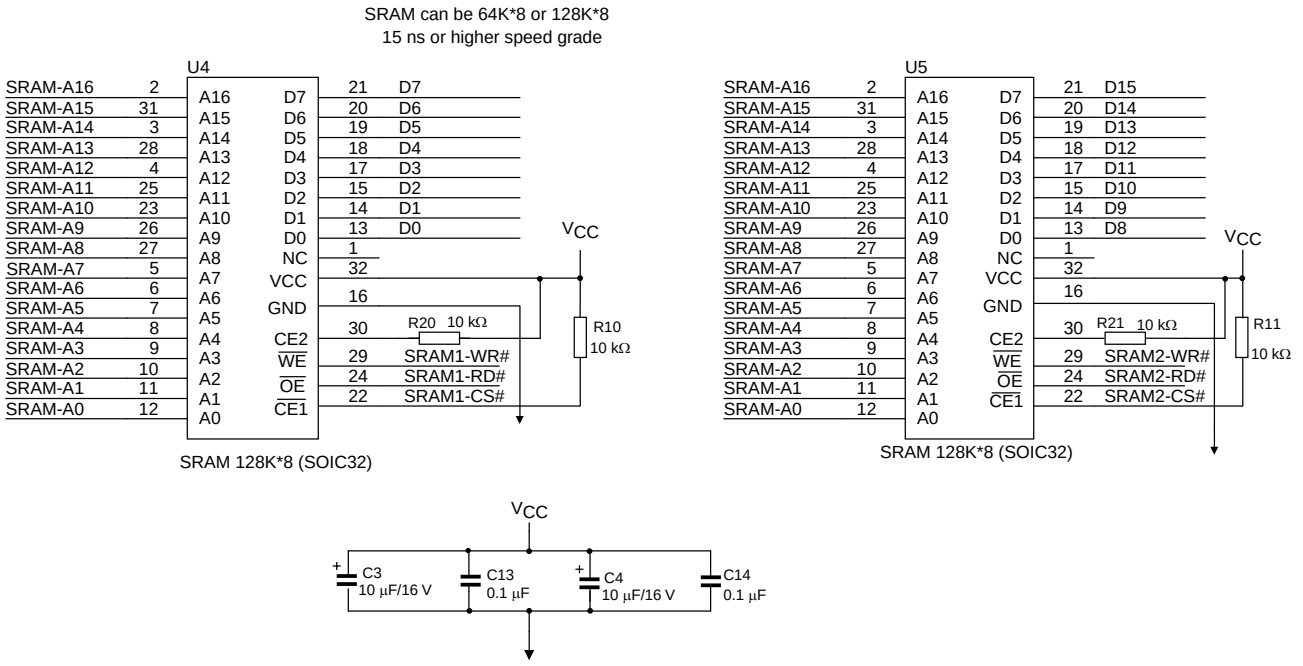

Fig 3. Schematics 2

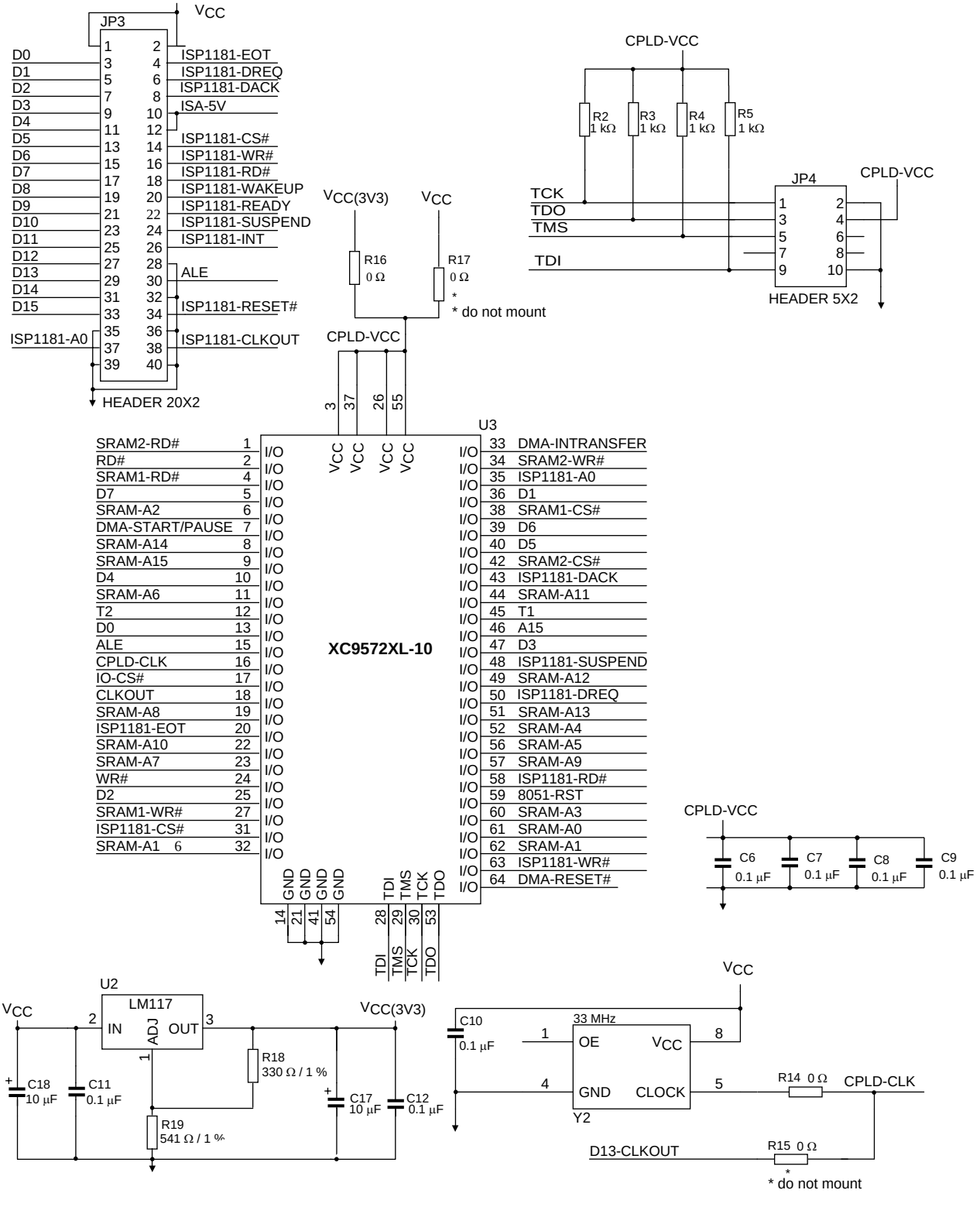

Fig 4. Schematics 3

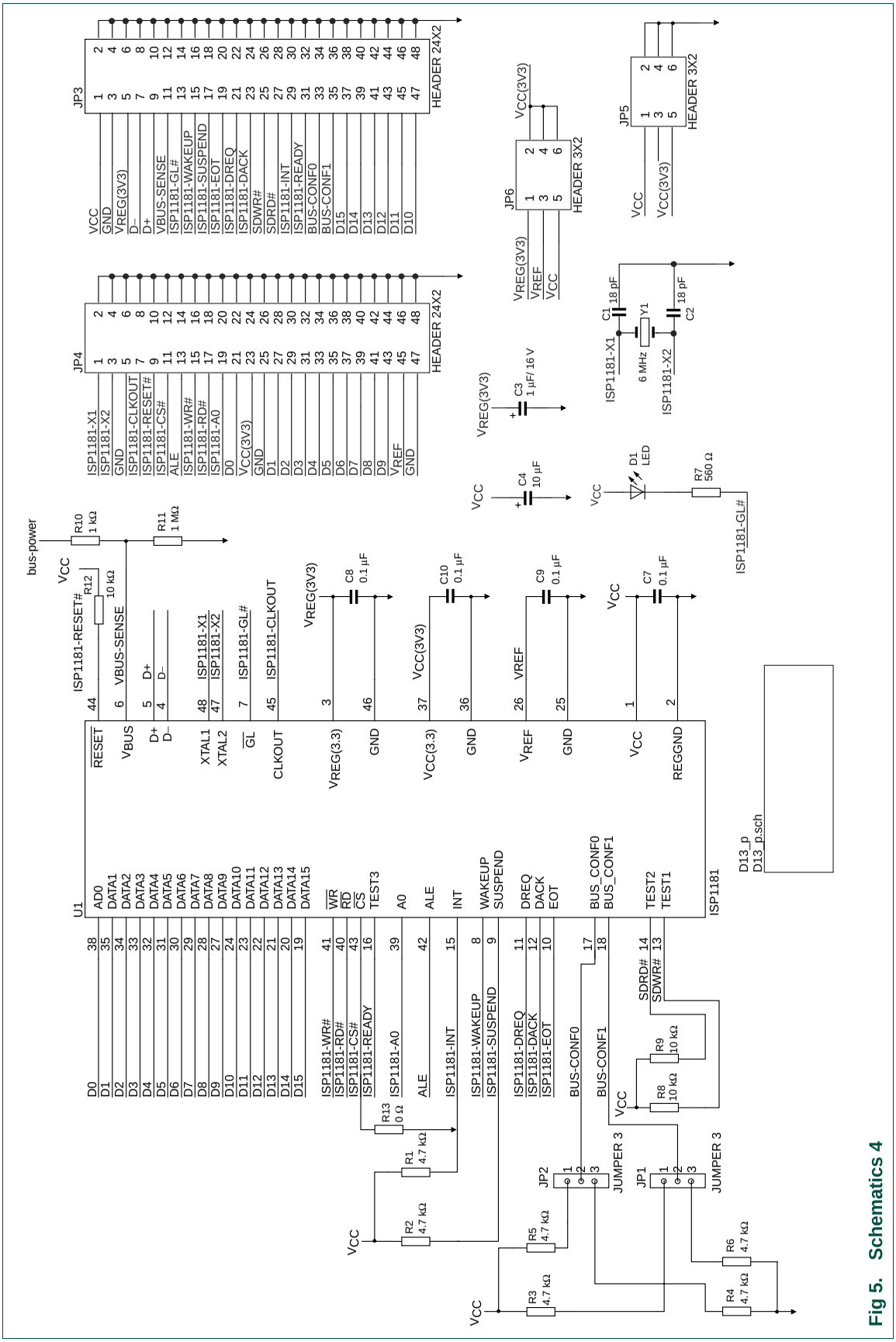

Fig 5. Schematics 4

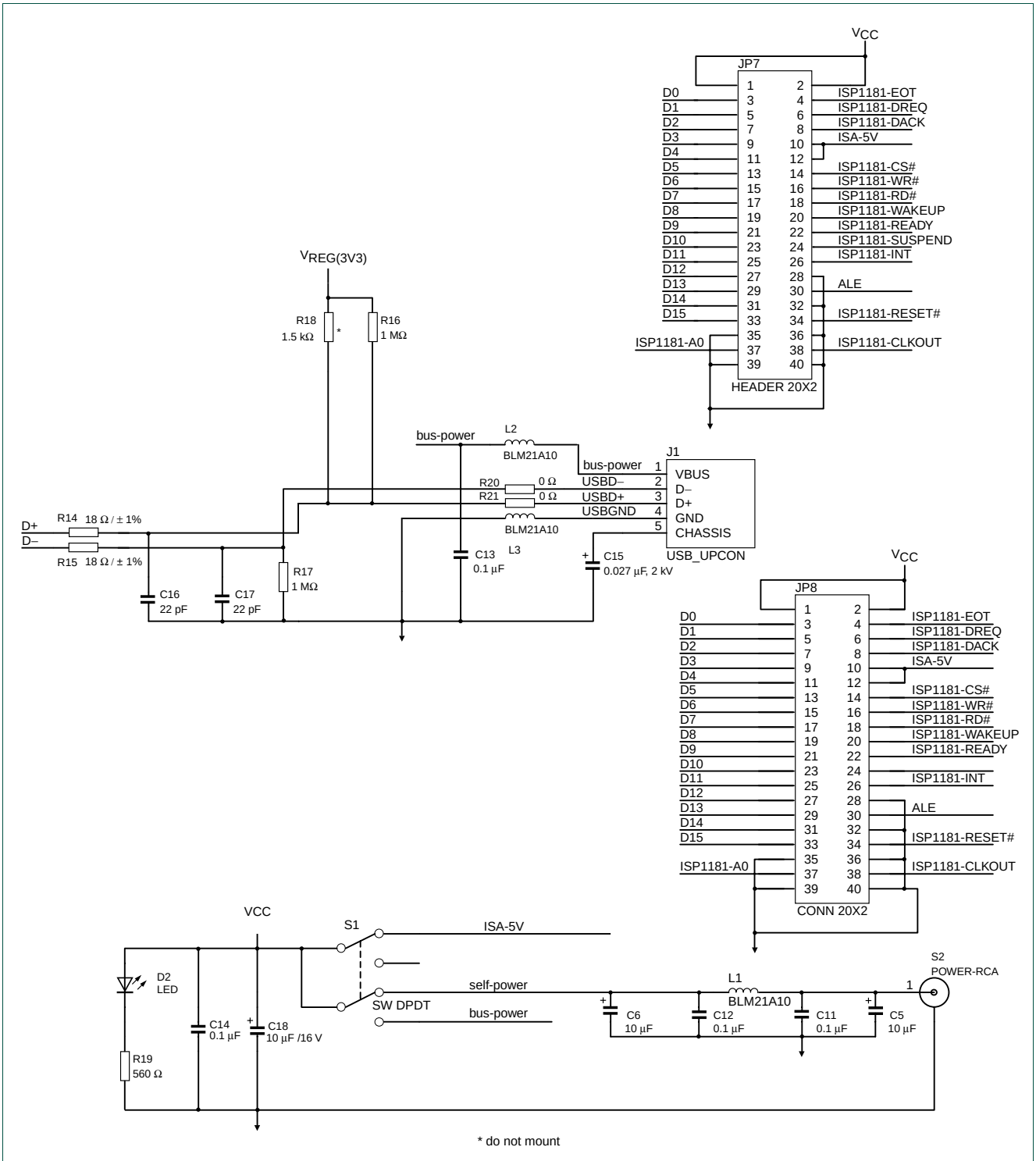

Fig 6. Schematics 5

8. References

- ISP1181A Full-speed Universal Serial Bus peripheral controller data sheet
- ISP1181B Full-speed Universal Serial Bus peripheral controller data sheet
- Universal Serial Bus Specification Rev. 2.0.

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